Paper 7, TDC Part-3 Chapter-3, Number Systems and Codes **Electronics 2'S Complement Airthmetic By: Mayank Mausam Assistant Professor (Guest Faculty) Department of Electronics** L.S. College, BRA Bihar University, **Muzaffarpur, Bihar**

• <u>2'S Complement Arithmetic : -</u>

To perform different types of arithmetic operation in digital system we need to design different digital circuits for each type of operation like addition, subtraction, multiplication and division. Designing so many digital circuits will make the system complex, costly and bulky. To get rid of this if we design such a circuit that can perform different operation by providing specific input.

So if it is possible to design such a circuit that can perform subtraction using digital circuit for addition.

Then the design of arithmetic circuit is cheaper and less bulky.

In 2's complement the subtraction is performed by adding the 2's complement representation of the subtrahend while addition of signed positive number is performed by the same method of addition.

Addition/Subtraction in 2's Complement

Addition/Subtraction of signed binary numbers can be performed conveniently using 2's complement representation of both the operands. So the method is used to perform addition/subtraction operation in digital systems.

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Binary Subtraction in 2's Complement

Subtraction in binary system is performed in following steps-

a) Add the 2's complement of the subtrahend to the minuend.

b) When the minuend is greater than the subtrahend, a carry is generated at the end of addition, discard the carry and the result is given by the remaining bits which is positive.

c) When the minuend is smaller than the subtrahend, no carry is generated at the end of addition, the answer is negative and is in 2's complement.

Let's see few example.

Examples on 2's complement based Sabtraction, using 8-but representation 64-39 25 complement sepresentation of +64 = 000000 complement representation of 0000000 Now. 64 - 32 = 64 + (-39)001 00

iscard Lexult is 0010000 -> (+32 2's complement representation a & complement representation of 2's complement representation of -00000

-64 = 32+ Now. 32-64 2 M 39 ne com Representation T men complement Represen T'm = 00 in 2's com +64

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Note: - a) When the 2 operands are of the opposite sign, the result is to be obtained by the rule of subtraction using 2's complement.

b) When the 2 operands are of the same sign, the sign bit of the result is to be compared with the sign bit of the operands. "If the sign bits are same", then the result is correct and is in 2's complement form.

"If the sign bits are not same", the result can't be accommodated using eight bits and the result is to be interpreted suitably. The result in this case will consist of nine bits (carry and eight bits), and the carry bit will give the sign of the number.

