⇒ Q.1 An AND gate is followed by a NOT gate using two inputs A & B find the Boolean exp" for the output (C).

Ans:- The AND-gate followed by NOT gate is shown in fig. 7.

As A & B are the two inputs of the AND gate, its output is AB which is the input of a NOT gate. Hence output of (AND-NOT) gates = $C = \overline{AB}$.

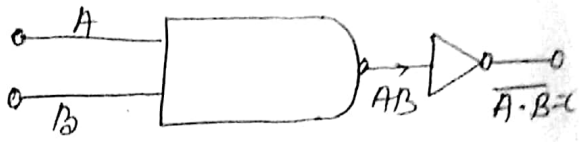

Fig. 7.

⇒ Q.2 Show how an OR-gate & an AND-gate can be constructed with NAND-gate.

see before fig. 6(b) & 6(c) for AND-gate & fig. 6(d) for OR-gate.

⇒ Explain how an OR-gate may be constructed with AND and NOT gates:-

Since AND-gate followed by NOT gate gives a NAND gate and by using 3 NAND-gates as shown in fig. 6(d) OR gate can be constructed.

⇒ Ex- Change the logic ckt fig. 8. into a simple on

Fig. 8.

A is the input of AND-gate and NOT-gate. Hence $\bar{A}$ & B are the inputs of OR gate. the output of OR-gate is therefore $\bar{A}+B$. this output is the another input of AND-gate whose output is $Y = A(\bar{A}+B)$.

This is modified as,

$A(\bar{A}+B) = A\bar{A}+AB = AB$ ($\because A\bar{A}=0$)

AB gives an AND gate with two inputs A & B shown as in fig 9.

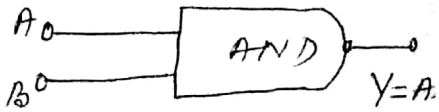

Fig. 9.